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International Bu

INTERNATIONAL APPLICATION PUBLISHED UNDER WO 9607971A1

(51) International Patent Classification 6 : G06F 13/38	A1	(11) International Publication Number: WO 96/07971
		(43) International Publication Date: 14 March 1996 (14.03.96)

(21) International Application Number: PCT/US95/10525

(22) International Filing Date: 17 August 1995 (17.08.95)

(30) Priority Data:
08/303,338 9 September 1994 (09.09.94) US

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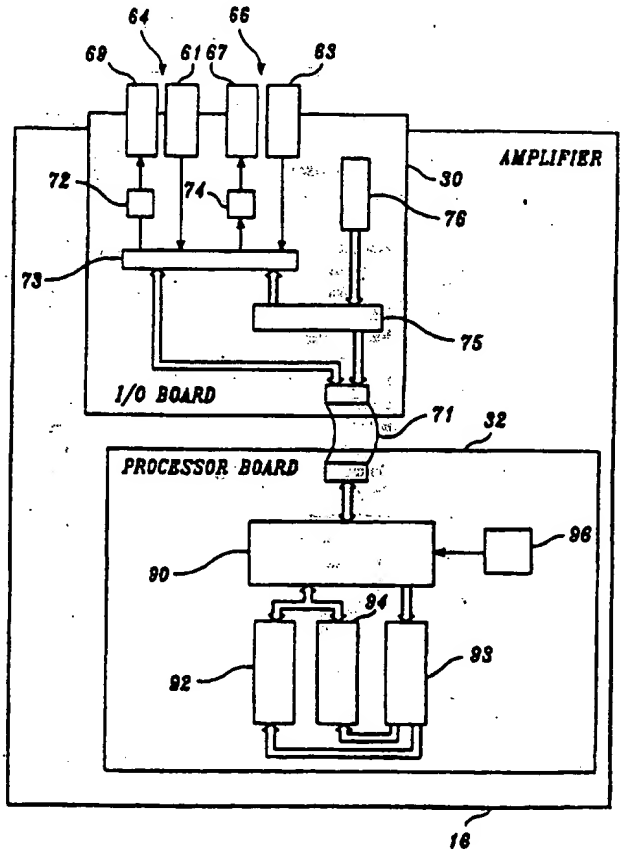
(81) Designated States: CA, JP, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: METHOD AND APPARATUS FOR AUTOMATICALLY CONFIGURING AN INTERFACE

(57) Abstract

Method and apparatus for allowing an electronic device (16) to communicate with one or more other electronic devices (14, 18, 22, 24, 52) via various communication protocols. The apparatus includes an I/O board (30) and a processor board (32). The I/O board (30) includes a plug (64, 66) for connecting to a particular type of transmission medium (10) and an electronic identifier (76) providing an identification of a first communication protocol with which the I/O board (30) is constructed to be used. The I/O board (30) and the processor board (32) are coupled together by a detachable connector (71). The processor board (32) includes a processor (90) and memory (90, 92). By disconnecting the I/O board (30) from the processor board (32), another I/O board (58) that is constructed to be used with a second communication protocol can be coupled to the processor board (32). The memory (90, 92) on the processor board (32) stores two units of program code (134, 136), one of which is used to communicate according to the first communication protocol and the other of which is used to communicate according to the second communication protocol. To automatically configure itself, the processor board (32) reads the electronic identifier (76) on the I/O board (32, 58) connected to the processor board (32), and based thereon selects the appropriate unit of program code (134, 136) so that the electronic device (16) communicates according to the specified communication protocol.



METHOD AND APPARATUS FOR AUTOMATICALLY CONFIGURING AN INTERFACE

Field of the Invention

This invention relates to methods and apparatus for interfacing an electronic device with one or more other electronic devices and, more particularly, methods and apparatus for providing a network interface or a point-to-point interface.

Background of the Invention

Electronic devices are being interconnected with increasing frequency. For example, in the music industry, amplifiers, equalizers, musical instruments, and various other devices are commonly interconnected to a control panel that can control the various devices. The various devices can also be interconnected to allow the devices to communicate with one another. Various transmission media such as fiber optic cables, coaxial cables, ribbon cables, and twisted wire pair cables can be used to interconnect electronic devices to allow the devices to communicate with one another. Furthermore, various communication protocols exist.

Typically, an interface card is included in an electronic device to allow the electronic device to communicate with other devices via a particular type of transmission medium and a particular communication protocol. That is, the interface card is constructed for use with a particular type of transmission medium and a particular type of communication protocol. As a result, if it is desired that an electronic device communicate via a different transmission medium or a different communication protocol than the one in use, the device's interface card must be changed to one dedicated to the desired type of transmission medium and communication protocol. Unfortunately, interface cards are expensive because typical

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various communication protocols is provided. The apparatus includes an I/O board and a processor board. The I/O board includes a plug, a driver, an electronic identifier, and a connector. The I/O board is connectable to a particular type of transmission medium via the plug. The driver is coupled to the plug for producing signals on the transmission medium. The electronic identifier provides an identification of a first communication protocol with which the I/O board is constructed to be used. The processor board includes a connector, memory, and a processor coupled to the memory and the connector. The processor board and I/O board are coupled together by connecting their connectors. Disconnecting the I/O board from the processor board allows another I/O board that is constructed to be used with a second communication protocol to be coupled to the processor board.

The memory on the processor board stores two units of program code, one of which is used to communicate according to the first communication protocol and the other of which is used to communicate according to the second communication protocol. The processor reads the electronic identifier on the I/O board connected to the processor board, and analyzes the identification provided by the electronic identifier to determine which of the two communication protocols is to be followed. The processor then selects the appropriate unit of program code in the memory, i.e., if the identification specifies the first communication protocol, the corresponding program code is selected. The processor executes this unit of program code so that the electronic device communicates with one or more other devices according to the specified communication protocol.

In accordance with further aspects of the invention, the first communication protocol is a bus network communication protocol and the second communication protocol is a point-to-point communication protocol. Furthermore, in one preferred embodiment of the invention, the I/O board that is constructed to be used with the first communication protocol is connectable to a fiber optic cable. The second I/O board that is constructed to be used with the second communication protocol is connectable to a RS232 cable.

In accordance with further aspects of the invention, the processor included on the processor board requires no program code from the I/O board.

In accordance with still further aspects of the invention, the electronic identifier comprises a dip switch.

In accordance with still further aspects of the invention, the identification provided by the electronic identifier on the I/O board also identifies the baud rate at which the I/O board is intended to be used. The processor on the processor board

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reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1 is a pictorial diagram of electronic devices interconnected in a bus network configuration with which the present invention can be used;

FIGURE 2 is a block diagram of the electronic devices and bus network shown in FIGURE 1;

FIGURE 3 is a block diagram representation of two electronic devices interconnected in a point-to-point configuration with which the present invention can be used;

FIGURE 4 is a block diagram of an amplifier including a processor board and an I/O board formed in accordance with the invention;

FIGURE 5 is a block diagram representation of a software/firmware paradigm that is preferably used in the processor board provided by the present invention; and

FIGURE 6 is a flow diagram of a method of automatically configuring the processor board based upon the I/O board that is connected to the processor board, in accordance with the invention.

Detailed Description of the Preferred Embodiment

FIGURES 1 and 2 illustrate a bus network 10 interconnecting various electronic devices 12 with which the present invention can be used so that they can be controlled by signals on the network. The electronic devices shown include two audio amplifiers 14, 16, an audio equalizer 18, and two personal computers 22, 24. Other devices necessary to a complete sound system and their interconnection to the illustrated devices are not shown since they do not form part of this invention.

As shown in FIGURE 2, the personal computers 22, 24 are connected to the bus network 10 by way of bridges 26. In contrast, the amplifiers 14, 16 and the equalizer 18 each include an I/O board 30 and a processor board 32 formed in accordance with the invention to allow the devices to be directly connected to the bus network 10. The I/O board 30 is specifically constructed for use with the bus network configuration and a particular type of transmission medium, whereas the processor board 32 can be used with different communication configurations and transmission media. The processor board 32 is coupled to the I/O board 30 by way of connectors so that the I/O board 30 can be easily connected to and disconnected from the processor board 32. By disconnecting the I/O board 30 from the processor board 32, another I/O board constructed for use with a different communication configuration and/or transmission media can be connected to the processor board 32.

appropriate function, possibly including sending a response packet back to the equalizer 18.

The processor boards 32 in the devices 14, 16, 18 are connected to other components in the devices to either control the devices directly or to control the devices in conjunction with other processors or controllers within the devices. For example, the amplifier 16 can include various analog electronics that are controlled by the processor board 32 based upon packets received over the bus network 10. Furthermore, while the processor board 32 is illustrated as a separate board, the components of the processor board 32 could be integrated into a larger board in the device, or the processor board 32 could be a section of a larger board.

The personal computers 22, 24 are not directly connected to the bus network 10. Rather, the personal computers 22, 24 are connected via RS232 interfaces 34 and the bridges 26. Standard personal computers typically include an RS232 card 36 for communicating with external devices such as printers. RS232 is an interface standard that specifies signal voltage levels, etc. RS232 is also a byte-level communication protocol that specifies start bits, stop bits, etc. for sending bytes of data. Generally, a higher level communication protocol is used on top of the RS232 byte-level communication protocol.

As show in FIGURE 2, the personal computers 22, 24 each include an RS232 interface card 36 and an RS232 cable 38. The personal computers 22, 24 also include software defining a point-to-point communication protocol that is used on top of the RS232 byte-level protocol. The bridges 26 provide the interface between the RS232 cables 38 and the bus network 10. Each bridge 26 includes a RS232 I/O card 40 for connecting to the RS232 cable 38, and a second I/O card 42 that is constructed for connecting to the transmission medium of the bus network 10. The bridges 26 include a bridge processor board 44 connected to each of the I/O boards 40, 42, to translate between the point-to-point communication protocol and the bus network communication protocol used on the bus network 10.

The bus network 10 shown in FIGURES 1 and 2 can be formed of various transmission media such as glass or plastic fiber optic cables, coaxial cables, twisted wire pair cables, ribbon cables, etc. In the music industry it is generally preferable to use fiber optic cables, as fiber optic cables are highly immune to electromagnetic interference and ground loops, and are capable of carrying signals over long distances without significant attenuation. As described herein, the bus network 10 represents fiber optic cables. Accordingly, the I/O board 30 shown in FIGURE 2 is constructed for use with fiber optic cables. As previously explained, the I/O board 30 can be

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This point-to-point communication protocol is referred to herein as the MediaWAN protocol.

With respect to FIGURE 3, the amplifier 50 includes the I/O board 58 and the processor board 32, which is identical to the processor boards 32 illustrated in FIGURE 2. The I/O board 58 is similar to the I/O boards 30 shown in FIGURE 2, except that the I/O board 58 is constructed for use with a RS232 cable. The processor board 32 included in the amplifier 50 controls the communication of the amplifier 50 using separate program code for communicating in accordance with the MediaWAN point-to-point communication protocol.

With respect to FIGURE 2, the bridge processor boards 44 include program code for both the MediaWAN point-to-point communication protocol and the MediaLink bus network communication protocol. The MediaWAN and MediaLink protocols are simultaneously used to provide the interface from the RS232 cables 38 to the bus network 10.

The amplifier 50 shown in FIGURE 3 can be connected to the bus network 10 illustrated in FIGURE 2 by simply replacing the I/O board 58 with an I/O board 30, which is constructed for use with the bus network 10. As briefly explained above and as explained in detail below, the processor board 32 includes hardware and program code so that the processor board automatically senses the type of communication protocol to use based upon an identifier on the I/O board that is connected to the processor board 32.

Processor Board and I/O Board

FIGURE 4 illustrates in greater detail the I/O board 30 and the processor board 32 in the amplifier 16 shown in FIGURES 1 and 2. The I/O board 30 includes two sets of plugs 64, 66, two drivers 72, 74, an electronic identifier 76, a shift register 75, and an application specific integrated circuit (ASIC) 73. The I/O board 30 is coupled to the processor board 32 by a ribbon cable 71. The processor board 32 includes a processor 90, an electronically erasable and programmable read-only memory (EEPROM) 92, a random access memory (RAM) 94, an application specific integrated circuit (ASIC) 73, and a timing clock (i.e., oscillator) 96.

With respect to the I/O board 30, the plugs 64, 66 are constructed to receive two fiber optic cables 68, 70, as shown in FIGURE 1. The drivers 72, 74 are respectively coupled to the plugs 64, 66 to produce light signals at the plugs to which the drivers are connected. The two sets of plugs 64, 66 are provided to allow the I/O board 30 to be used on a bus network 10, as illustrated in block diagram form in FIGURE 2. With fiber optic cables it is generally not possible to tap off of the cable.

register 75 is used to allow a serial control line of the processor 90 to control the ASIC 73, which requires parallel control lines. For example, in one preferred embodiment, the ASIC 73 requires four parallel lines (bits) to select its mode. The shift register 75 shifts four bits sent over the serial control line of the process 90 into four bits, which are applied to the ASIC 73.

The electronic identifier 76 included on the I/O board 30 identifies the communication protocol and the baud rate with which the I/O board 30 is constructed to be used. In one preferred embodiment, the electronic identifier 76 is a dip switch set to identify the baud rate and the communication protocol. However, those skilled in the pertinent art will readily recognize that other devices could easily be used to serve as the identifier 76. For example, the electronic identifier 76 could be formed of electronic circuitry wired to uniquely identify the baud rate and communication protocol. The identifier 76 could also be formed of a small memory device storing one or more bytes of data to uniquely identify the baud rate and communication protocol. With respect to the use of a dip switch for the electronic identifier 76, multiple pins on the dip switch must be read to determine the identification provided by the dip switch. The shift register 75 is connected to these pins, and converts the parallel data into serial data that is sent to the processor 90.

In one preferred embodiment, one end of the ribbon cable 71 is secured to the processor board 32 and the I/O board 30 includes a connector to which the other end of the ribbon cable 71 can be connected. The ribbon connector 71 can be disconnected from the I/O board 30, so that a different I/O board can be connected to the processor board 32. In one preferred embodiment of the invention, at least two types of I/O boards are provided, one for use with a bus network communication protocol (e.g., the MediaLink protocol) and the other for use with a point-to-point communication protocol (e.g., the MediaWAN protocol). The I/O board 30 shown in FIGURE 4 is constructed for use with a bus network communication protocol at a 125k baud rate, with the bus network 10 formed of fiber optic cables.

The I/O board 58 shown in FIGURE 3 is constructed for use with a point-to-point communication protocol, with the transmission medium formed of the RS232 cable 54. The I/O board 58 contains the same basic components as the I/O board 30, except as follows. The I/O board 58 has a single plug 82, to which the RS232 cable 54 is connected. Because there is only a single plug 82, the I/O board 58 includes only one driver 84 (a RS232 driver), which is connected to the plug. As with respect to the I/O board 30, the I/O board 58 includes a shift register 81 and an ASIC 83, and is connected to the processor board 32 by a ribbon cable 87. The I/O

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level. Such persons will also readily know how to interconnect the various components at the circuit level. Accordingly, to avoid unduly complicating the present disclosure, these details are omitted.

Bridge

The circuitry of the bridges 26 illustrated in block diagram form in FIGURE 2 includes many of the same components as the processor board 32 and the I/O cards 30, 58. The bridge processor board 44 includes a processor chip 100, e.g., one of the HC11 family of Motorola processors. The bridge processor board 44 also includes a timing clock 102, a RAM 104, and a EEPROM 106. The I/O board 42 is similar in structure to the I/O board 30, and the I/O board 40 is similar in structure to the I/O board 58. Each of the I/O boards 40, 42 include appropriate plugs for connecting to the type of external cable to which they are intended to be connected. The I/O board 42 includes fiber optic cable plugs for connecting to the bus network 10, and the I/O board 40 has an RS232 plug for connecting to the RS232 cable 38. The I/O board 40 includes a RS232 driver 108, and the I/O board 42 includes two fiber drivers 110 and 112. The processor chip 100 includes a UART port that is used to send and receive serial data from the I/O board 42. The bridge processor board 44 also includes an external UART (not shown) for sending and receiving serial data from the I/O board 40.

The I/O boards 40, 42 also include electronic identifiers (not shown) to identify the transmission medium and communication protocol with which the I/O boards 40, 42 are intended to be used. At start-up initialization of the bridge 26, the bridge processor board 44 determines the type of I/O boards present and selects the appropriate program code, as described with respect to the processor board 30. To make the bridge 26 compatible with a different transmission medium and/or communication protocol, the I/O board 40, 42 could be replaced with appropriate I/O boards. As is the case with respect to the processor board 32 and I/O board 30 shown in FIGURE 4, the circuit-level implementation of the bridge can be carried out in various ways, as will be readily appreciated by those skilled in the pertinent art.

Program Code Paradigm

FIGURE 5 illustrates the organization of the program code within one preferred embodiment of the processor board 32 shown in FIGURE 4. The program code is organized into units (referred to herein as SoftSlots) in the ROM in the processor 90 and in the EEPROM 92. The SoftSlots 120, 122 are based in part upon the object-oriented programming paradigm in that each SoftSlot 120, 122 is a class defining variables and methods (i.e., functions). Instances, i.e., objects, of each

The PACKET SoftSlot 130 provides variables and methods that define packets, which are the unit of information communicated between devices in the MediaLink and MediaWAN communication protocols. The PACKET SoftSlot is a child of the EVENT SoftSlot, so that packets are events that control the execution of themselves. The PACKET SoftSlot 130 points to the UART SoftSlot 132, which defines variables and methods for controlling the UART within the processor 90. The UART SoftSlot is a child of the IO Port SoftSlot.

The UART SoftSlot 132 points to the MEDIALINK SoftSlot 134, which in turn points to the MEDIAWAN SoftSlot 136. The MEDIALINK SoftSlot provides variables and methods that define the MediaLink bus network communication protocol, and the MEDIAWAN SoftSlot provides variables and methods that define the MediaWAN point-to-point communication protocol, supporting a 125k baud rate, a 9600 baud rate and other baud rates. The MEDIALINK and MEDIAWAN SoftSlots 134, 136 are each a child of the IO Port SoftSlot.

The MEDIAWAN SoftSlot 136 points to the Virtual Device Management (VDM) SoftSlot 138, which is a child of the TAPCORE SoftSlot. The VDM SoftSlot 138 provides variables and methods that identify the type of device, e.g., an amplifier, that the processor board 32 is housed in, and the VDM SoftSlot 138 provides methods that allow the device to identify itself when queried by other devices. The VDM SoftSlot 138 also provides methods that allow the processor 90 to write to the RAM 94 and program the EEPROM 92 on the processor board 32.

The VDM SoftSlot 138 points to the NULL APP SoftSlot 140, which is the last SoftSlot within the processor 90. The NULL APP SoftSlot 140 is a child of the TAPCORE SoftSlot and provides variables and methods that define a generic device. The functionality and identity of the device in which the processor board 32 is housed is defined by the NULL APP SoftSlot, unless there is one or more APPLICATION SoftSlots 122 within the EEPROM 92. The NULL APP SoftSlot reads the identifier on the I/O board 30, and based thereon selects either the bus network protocol defined by the MEDIALINK SoftSlot 134 or the point-to-point communication protocol provided by the MEDIAWAN SoftSlot 136, as described below.

The NULL APP SoftSlot 140 points to the first APPLICATION SoftSlot 142 in the EEPROM 92, if there is one. More particularly, the NULL APP SoftSlot 140 points to a memory location in the EEPROM 92 that points (i.e., contains the memory address location) of the first APPLICATION SoftSlot 142; the bytes at this memory location are referred to herein as link bytes. If there are no APPLICATION SoftSlots or any other SoftSlots in the EEPROM 92, the link bytes contain zeros. In this case,

rate, depending on that specified by the identifier 80 on the I/O board 58. After locating the appropriate SoftSlot, program code contained within the SoftSlot is activated, as indicated at the block 160.

Any remaining initialization steps 162 specified by subsequent SoftSlots in the linked-list are then performed. After the start-up initialization is completed, the device runs according to the activated program code contained within the SoftSlots.

While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention. For example, while the processor board 32 described above only contained SoftSlots for two communication protocols, additional communication protocols can be readily supported by including additional SoftSlots in the processor board 32, in the ROM in the processor 90, in the EEPROM 92, or in some other memory device. The electronic identifier on an I/O board would identify which of the communication protocols is to be used. Furthermore, while only the fiber optic I/O board 30 was described for use with the bus network 10, various other I/O boards could be used if a transmission medium other than fiber optics is used for the bus network 10. In this case, if the processor board 32 must interact differently with different types of I/O boards for different transmission media, the SoftSlots would contain appropriate program code for each of the I/O board types for the various bus network transmission media. For example, if an I/O board constructed for a bus network formed of coaxial cables is used, the processor board 32 may require a different type of initialization. The electronic identifier on the I/O board would identify the type of transmission medium, and the processor board 32 would select the appropriate SoftSlot program code for the transmission medium type. Furthermore, configuration in addition to that previously described could be performed based upon the identification provided by the electronic identifier 76. For example, it is possible that a particular I/O board is to be used with various electronic identifier settings. In this case, the I/O board would configure itself based upon the electronic identifier setting. Hence, within the scope of the appended claims, it is to be understood that the invention can be practiced otherwise than as specifically described herein.

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executing said one of said first and second units of program code so that said device communicates with said one or more other devices according to said first communication protocol.

2. The apparatus of Claim 1, wherein said processor requires no program code from said I/O board.

3. The apparatus of Claim 1, wherein:

said identification provided by said electronic identifier on said I/O board also identifies a baud rate at which said I/O board is intended to be used;

said processor analyzes said identification to determine said baud rate; and

said processor executes said one of said first and second units of program code so that said device communicates with said one or more other devices according to said first communication protocol at said baud rate.

4. The apparatus of Claim 1, wherein said second connector is detachably connected to said first connector so that said I/O board can be disconnected from said processor board and a second I/O board constructed to be used with a second communication protocol can be coupled to said processor board, said second I/O board including a second electronic identifier providing a second identification of said second communication protocol.

5. The apparatus of Claim 4, wherein said particular type of transmission medium to which said plug of said I/O board is connectable comprises a fiber optic cable, and wherein said second I/O board is formed to be used with a second type of transmission medium comprising a RS232 cable.

6. The apparatus of Claim 1, wherein said electronic identifier comprises a dip switch.

7. The apparatus of Claim 1, wherein said first communication protocol is a bus network communication protocol and said second communication protocol is a point-to-point communication protocol.

8. A method of automatically configuring an electronic device for communicating with one or more other electronic devices via various communication protocols, said electronic device detachably connected to an I/O board constructed to

12. The method of Claim 8, wherein said first communication protocol is a bus network communication protocol and said second communication protocol is a point-to-point communication protocol.

13. A processor board that automatically configures itself for allowing an electronic device to communicate with one or more other electronic devices via various communication protocols, said processor board comprising:

(a) a connector detachably connectable to an I/O board to couple said I/O board to said processor board, said I/O board being constructed to be connected to a particular type of transmission medium for use with a first communication protocol, said I/O board including an electronic identifier providing an identification of said first communication protocol;

(b) memory storing first and second units of program code, one of which is used to communicate according to said first communication protocol and the other of which is used to communicate according to a second communication protocol; and

(c) a processor coupled to said memory and said connector, said processor for:

(i) reading said electronic identifier on said I/O board to determine said identification;

(ii) analyzing said identification to determine which of said first and second communication protocols is to be followed;

(iii) selecting one of said first and seconds units of program code to communicate according to said first communication protocol; and

(iv) executing said one of said first and second units of program code so that said electronic device communicates with said one or more other devices according to said first communication protocol.

14. The processor board of Claim 13, wherein said processor requires no program code from said I/O board.

15. The processor board of Claim 13, wherein:

said identification provided by said electronic identifier on said I/O board also identifies a baud rate at which said I/O board is intended to be used;

said processor analyzes said identification to determine said baud rate; and

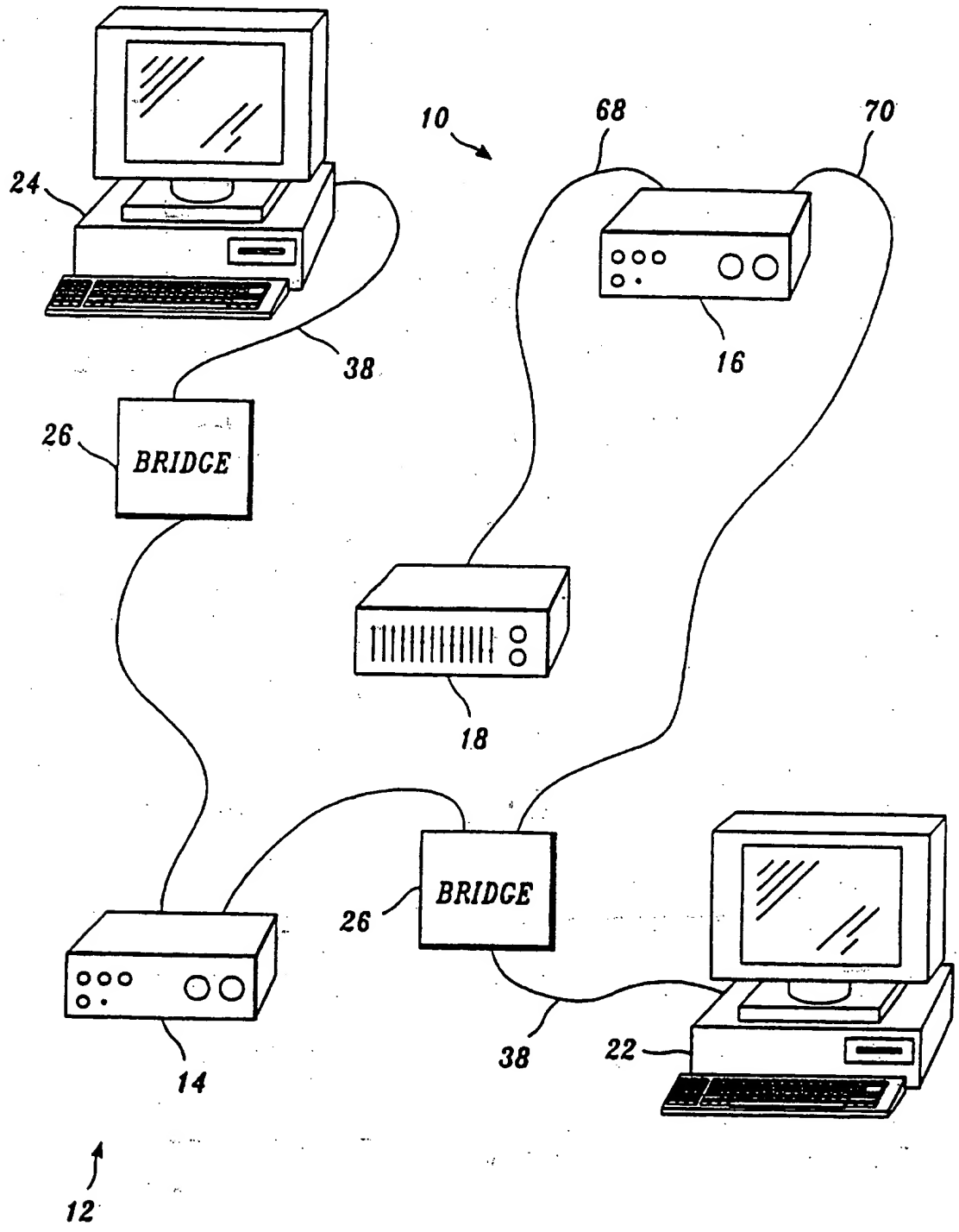


Fig. 1.

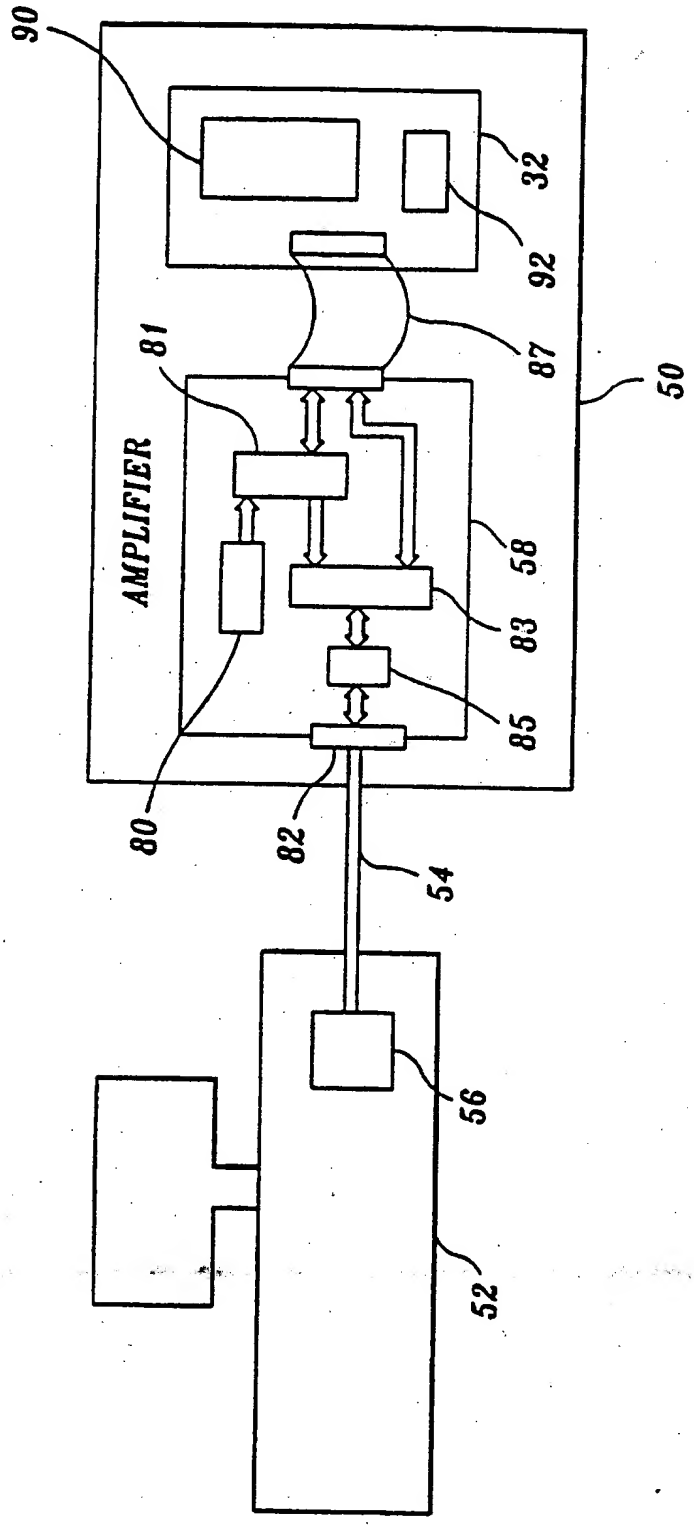
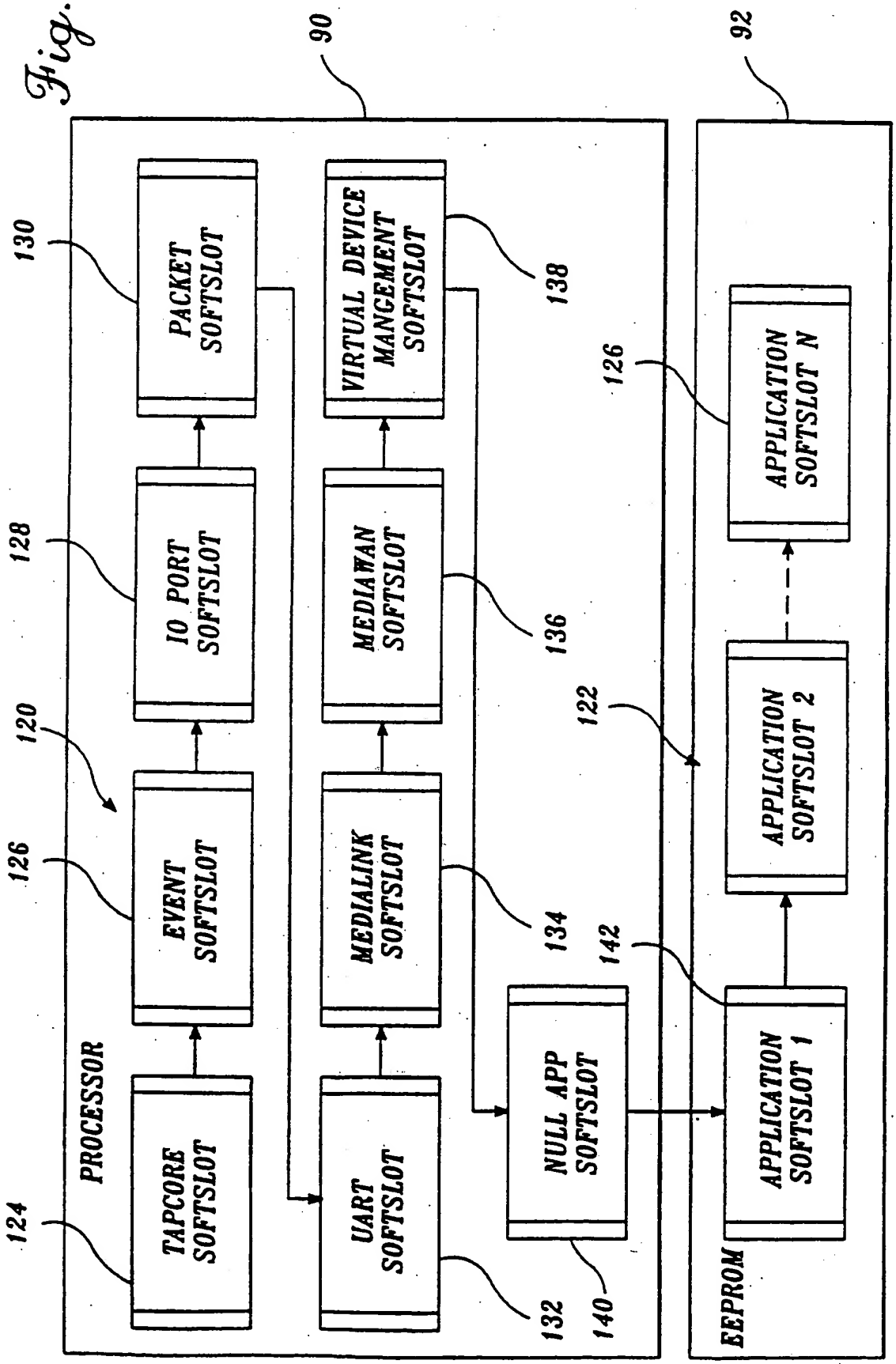


Fig. 3.

Fig. 5.



BNSDOCID: <WO 9607971A1>

INTERNATIONAL SEARCH REPORT

Inter. nal Application No
PCT/US 95/10525

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F13/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,4 322 792 (BURROUGHS) 30 March 1982 see column 4, line 17 - line 45; figure 3 see column 6, line 37 - line 48	1-4,7,8, 10,11, 13,14,16
A	US,A,4 281 315 (BELL TELEPHONE) 28 July 1981 see abstract; claim 1 see column 13, line 55 - line 64; figures 1,2	1,8,13
A	US,A,4 775 931 (HEWLETT-PACKARD) 4 October 1988 see column 1, line 39 - line 50	1,3,4,6, 8-11,13, 15,16

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
8 January 1996	26.01.96

Name and mailing address of the ISA	Authorized officer
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Form PCT/ISA/210 (second sheet) (July 1992)

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